REMARKS/ARGUMENTS

Prior to this amendment, claims 1-15, 20-34, 36 and 37 were pending. In this amendment, claims 1, 20, and 36 are amended. No claims are canceled or added. Thus, after entry of this amendment, claims 1-15, 20-34, 36, and 37 remain pending.

Interview

Applicants would like to thank the Examiner for extending the courtesy of a telephone interview with counsel, David B. Raczkowski, on November 7, 2008 where differences in the amended claims from the cited references were discussed.

Rejections under 35 USC § 103(a), Leaver in view of Cong

Claims 1-9, 20-28 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. (US Patent No. 6,195,788) in view of Cong et al. ("Cut Ranking and Pruning: Enabling a General and Efficient FPGA Mapping Solution").

Claim 1

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *wherein the fixed-configuration secondary hardware has a plurality of inputs, the inputs common to at least two of the programmable logic elements, the method comprising:*
> *for each of a plurality of portions of the user design, determining ...one or more sets of input assignments of signals in the user design to the fixed-configuration secondary hardware, each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware;*
> *ranking ...the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware;*
> *selecting ... the a highest ranked set of input assignments, wherein the highest ranked set is assigned to the fixed-configuration secondary hardware at least two or more times.*

In the advisory action, the Office Action asserts that the I/O pins 302 are the fixed-configuration secondary hardware. *See Leaver*, FIG. 3 and col. 9 lines 48-60. The I/O pin is the input to a logic node 304. *Id.* However, an I/O pin does not itself have an input.

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Accordingly, the proposed combination does not teach or suggest "*wherein the fixed-configuration secondary hardware has a plurality of inputs*," as recited in claim 1

Also, an I/O pin does not perform any type of logic function. Thus, regardless of the signals that are provided to a group of I/O pins, these I/O pins do not "*provid[e] an implementation of a logic function of [a] portion of the user design*," as recited in claim 1.

Furthermore, the Examiner has still <u>never addressed</u> that Table 1 of Leaver provides the relative cost of using a PTERM versus a LUT, and <u>not</u> a ranking of the I/O pins or the assignments of signals to these I/O pins. No explanation has been provided for how the relative cost of mapping of a logic cone to a PTERM or a LUT ranks sets of signals that are assigned to a logic cone. Applicants formally request an explanation if this interpretation is to be maintained.

Additionally, the Advisory Action asserts that Cong teaches ranking cuts based on whether a cut represents lesser nodes and the greater number of shared nodes. <u>This is incorrect</u>. The cuts are ranked based on whether a cut results in a smaller mapped area, when the portions created by the cut are mapped to the circuit. *See Cong*, section 3.2. A smaller mapped area is <u>not</u> equivalent to lesser nodes. As section 3.3.5 of Cong points out, there is a trade off in the mapped area for less nodes when the mapping is done. Therefore, in some instances, lesser nodes may result in a greater total mapped area.

Since the ranking is not based on the number of nodes of a cut, then the ranking is <u>not</u> for the input assignment associated with a node, as is asserted in the Advisory Action.

Moreover, Cong never mentions assigning any signals to inputs of a node. Even if such an assignment were inherent, only <u>one assignment</u> would be involved. Thus, the number of times an assignment is made would never used in a ranking, i.e. all would be of equal rank. Accordingly, the combination does not teach or suggest "*<u>ranking ...the sets</u> of input assignments by determining a <u>number of times</u> each <u>set is assigned</u> to the fixed-configuration secondary hardware*" and "*selecting ... the a highest ranked set of input assignments, wherein the highest ranked set is assigned to the fixed-configuration secondary hardware at least <u>two or more times</u>.*"

For at least these reasons, claim 1 and its dependent claims are allowable of these references. Support for amendments to claim 1 can be found, for example, in paragraphs 39-43.

Claim 20

Applicants submit that claim and its dependent claims are allowable for at least the same reasons as claim 1.

Claim 36

Claim 36 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 36. For example, claim 36 recites:

> *the integrated circuit comprising a plurality of programmable logic elements, each programmable logic element comprising a register, a lookup table, and a plurality of logic gates having a plurality of inputs ...*
>> *for each register in the plurality of registers in the user design...:*
>>> *determining a logic representation for each of one or more groups of at least one logic gate having a plurality of inputs, the at least one logic gate coupled to the input of the register in the user design;*
>>> *determining at least one way to implement each logic representation using the plurality of logic gates in a programmable logic element.*

At page 5, the Office Action states that FIG. 1C shows the logic gates of both the user design *and* the integrated circuit. However, FIG. 1C shows a logic element of only the resulting programmable logic device 100, and *not* also of the user design. *See Leaver*, col. 4 line 53 to col. 5 line 7

Since FIG. 1 C does not show logic gates of both the user design and the integrated circuit, the combination does not teach or suggest "*determining at least one way to implement the logic representation [of the logic gates in the user design] using the plurality of logic gates in a programmable logic element,*" as recited in claim 36.

Furthermore, FIG. 1C shows a <u>LUT</u> and a <u>register</u>, but does <u>not</u> show a plurality of logic gates. Therefore, the combination does not teach or suggest "*each programmable logic*

element comprising a register, a lookup table, and a plurality of logic gates having a plurality of inputs." Support for this claims element can be found, for example, in FIG. 2.

Additionally, as described above, Cong does not mention assigning input signals to a node. Note the relationship of $K1 < K2 < Kc$ simply states that there are LUTs of different input sizes. *See Cong*, section 3.3.5. The statement has nothing to do with the assignment of signals to the inputs of the LUTs, but just the number of inputs that exist in the LUTs.

Thus, there are no particular assignment of signals to any of the inputs of the LUTs, nor are the assignments counted or ranked. Accordingly, the combination does not teach or suggest *"determining a first input signal and a first input of the logic gates in the programmable logic elements, wherein the first input signal is assigned to the first input more than other input signals are assigned to an input of the logic gates in the programmable logic elements,"* as recited in claim 36.

For at least these reasons, claim 36 and its dependent claims are allowable of these references. Support for amendments to claim 36 can be found, e.g., in paragraphs 39-43.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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